CIRCUIT AND METHOD FOR TURN-ON OF AN INTERNAL VOLTAGE RAIL

FIELD OF THE INVENTION

The present invention relates to electronic circuitry and, in particular, to a circuit for turning on an internal voltage rail.

BACKGROUND OF THE INVENTION

Most prior art solutions, for current and voltage control during turn-on of a voltage source, limit current to a large switching transistor through a resistor or current source to the switching transistor. Some have additional capacitance to the source or drain to further slow the switching. However, this results in a constantly rising gate voltage, which does not allow for ideal turn on characteristics of the transistor. An alternative splits up the transistor into smaller sizes, and turns on one or more smaller transistors, and leaves the majority of the transistor off until the supply reaches its operating voltage. This has risks associated with the initial current spike that occurs through only a small part of the transistor area, causing electromigration and reliability risks.

SUMMARY OF THE INVENTION

A circuit and method for turning on an internal voltage rail includes: coupling a first transistor between a power supply node and an internal voltage rail node; mirroring a current from a second transistor to the first transistor during a turn-on time period; and coupling a control node of the first transistor to a bias voltage node after the turn-on time period. This solution permits current controlled turn-on of the first transistor, but a fully switched-on first transistor once turn-on is complete.

BRIEF DESCRIPTION OF THE DRAWINGS

In the drawings:

FIG. 1 is a schematic of a preferred embodiment circuit for turning on an internal voltage rail;

FIG. 2 is a plot of the inputs for the circuit of FIG. 2.

DETAILED DESCRIPTION OF PREFERRED EMBODIMENTS

The solution according to the present invention permits current controlled turn-on of the transistor, but a fully switched-on transistor once turn-on is complete. A preferred embodiment circuit schematic is shown in Figure 1. The circuit of Figure 1 includes transistors M1 (PMOS), M2 (PMOS), M3 (NMOS), M4 (PMOS), and M5 (PMOS); internal circuitry 20; inverters 22 and 24; buffer 26; source voltages VDD and VSS; nodes N1-N5; internal voltage rail 28; and inputs IN1, IN2, and IN3. A plot of the inputs IN1, IN2, and IN3 is shown in Figure 2.

The mode of operation is as follows: In the off state transistor M5 is off. This is achieved by input IN1 being high, forcing node N1 low and node N5, the gate of transistor M5, high, while input IN3 is low, forcing node N3 low and holding off transistor M3. The state of input IN2 can be either low or high, but might be preferentially low to force transistor M4 into the 'off' state for reduced off-state leakage. Since transistor M5 is off, the internal voltage rail floats low.

In order to turn the internal circuitry 20 on, transistor M5 is turned on. This is achieved by turning on transistor M3, a current controlled transistor (long channel; narrow width transistor, or a transistor in series with a current controlling element such as a resistor or current source). It is standard

procedure to control turn on of a large transistor through controlled current supply, thus providing an RC or C/I time constant. However, this does not necessarily provide the most accurate time constants over temperature, and a controlled current turn-on is used in this invention. Transistor M3 is turned on, and transistor M1 is turned off. Also, transistor M4 is turned on (or remains on). This allows the mirroring of current between transistors M2 and M5, providing a controlled turn on of the internal rail voltage 28. Once the internal rail has turned on, transistor M4 is turned off, and the voltage at node N5 falls from a Vt (threshold voltage) below supply VDD to ground VSS, permitting full performance of transistor M5. If transistor M4 is turned off prematurely, transistor M5 will pull up rapidly at full strength.

While this invention has been described with reference to an illustrative embodiment, this description is not intended to be construed in a limiting sense. Various modifications and combinations of the illustrative embodiment, as well as other embodiments of the invention, will be apparent to persons skilled in the art upon reference to the description. It is therefore intended that the appended claims encompass any such modifications or embodiments.